Ohmic Contact of Cu/Mo and Cu/Ti Thin Layers on Multi-Crystalline Silicon Substrates

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ABSTRACT: *Cu-Mo and Cu-Ti contact structures were fabricated on multi-crystalline silicon substrates to provide a low resistance ohmic contact. Deposition steps are done in an excellent vacuum chamber by means of electron beam evaporation and samples are then annealed for the realization of an efficient alloy layer. The effects of process parameters such as film thickness, annealing duration and temperature on the contact quality have been investigated and optimized for achieving the best special contact resistivity. The specific contact resistance obtained for Cu-Mo and Cu-Ti structures were 8.58×10^{-6} Ω-cm^2 and 9.72×10^{-6} Ω-cm^2, respectively. Finally, between the two proposed structures a comparison has been made which is resulted in the selection of Cu-Mo contact as the better structure due to its less resistance and better adhesion to the substrate.*

KEY WORDS: *Cu-Mo contact, Cu-Ti contact, Ohmic contact, Resistivity.*

INTRODUCTION

Recently, due to high cost reduction potential, multi-crystalline silicon substrate have been considered as an attractive choice for commercial solar cells [1-3]. The solar conversion efficiencies of commercial mc-cells have been obtained up to 17% [4]. There have been many attempts to obtain high quality and low resistance ohmic contacts to silicon solar cells [5-7]. One of the important issues about the Solar Cells is their metal contacts which must have a good adhesion and low resistivity. For achieving these goals, many structures have been examined on the normal single-crystalline wafers [8].

In this paper, we consider for the first time a stack of Cu-Mo and Cu-Ti thin films on multi-crystalline n-type silicon wafers for solar cell applications. However, these structures have been studied for their possible application as interconnect in Very Large Scale integration (VLSI) circuits [9]. We believe that these two structures annealed at a proper temperature can form a high quality and low resistance alloy with a perfect contact interface [9]. In section 2, we explain our experimental steps including preparation of the wafers, cleaning and texturing their surfaces, deposition of the layers, annealing and

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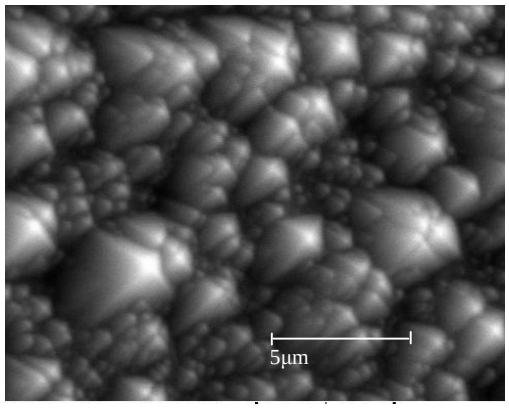
measurement formation. Section 3 considers the effect of various process parameters, especially the annealing temperature, on the contact quality. Finally, in section 4, a summary of this work is presented.

EXPERIMENTAL

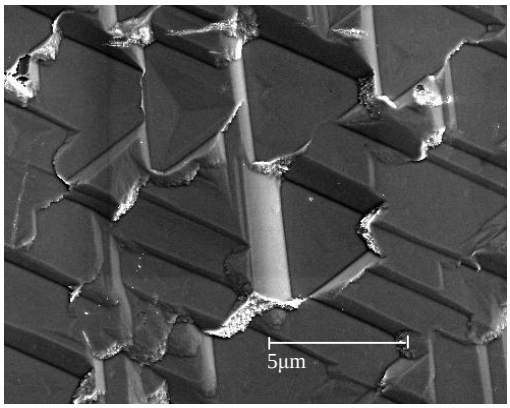
The substrate is a p-type multi-crystalline silicon wafer with a doping density of about $1\times10^{17}cm^{-3}$. First, the surface of this wafer is doped n-type by the diffusion of the phosphorus for achieving a concentration of about $8\times10^{18}cm^{-3}$ with an efficient depth of 0.5 μm. This profile is produced by using the Chemical Vapor Deposition (CVD: ASM diffusion furnace 4 stack 100 mm diameter) method. Substrates are exposed to a mixture flow of Ar, $POCl_3$ (The inert Ar gas passes through a bubbler containing $POCl_3$ and so carrying phosphorous components into the oven), N_2 and O_2 in the oven at the temperature of 900 °C for 15 minutes. The next step is the wafer texturing which reduces the surface reflectance and increases the quantum efficiency in solar cells. Many efficient techniques have been suggested for creating neat textures to minimize surface reflection [10-13]. As we were more interested in contact quality, we preferred the simple method of using anisotropic KOH solution for this purpose. As can be seen in the SEM pictures of Fig. 1, different surface profiles have been obtained for different crystal directions in unlike regions of the multi-crystalline wafers. The duration of laying samples in KOH solution was adjusted so that in all regions an acceptable level of roughness can be observed.

The samples were then RCA cleaned, treated in 10% HF solution to achieve the best interface, rinsed in deionized (DI) water, blown dry by N_2 and immediately loaded into the deposition chamber.

Then by means of electron beam (Veeco: Model AVC-1000), different thicknesses of Ti or Mo and then Cu have been deposited at a temperature of about 100 °C and at the vacuum of 2×10^{-6} Torr. Then the samples have been patterned by UV lithography method and finally annealed in an oven under various temperatures and durations for formation of the desired alloy and ohmic contact. For extracting the contact resistance and the sheet resistance of the doped silicon and the transmission line model, we used the TLM method (which is the suggested method for this extraction especially at low temperatures) [14,15]. Fig. 2 shows the pattern we



(a)



(b)

Fig. 1: SEM image of the surface profile of a textured sample. a) pyramids are formed in the <100> direction regions of the sample where the duration of KOH exposure was short. b) after a short time some steps can be observed in the <111> direction regions.

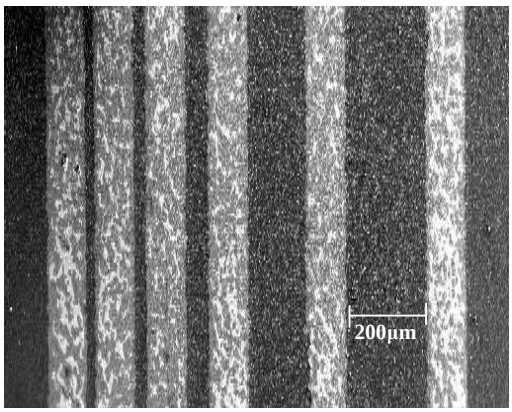


Fig. 2: SEM image of a sample after the annealing and the lithography process. The metal alloy has been patterned with a mask designed for the realization of the TLM method.

have provided for using this method. The total resistance R_T of the metal/semiconductor system is $R_T = 2R_C + 2R_M + R_{SEM}$ where R_M is the resistance of the metal (here mixture of Cu-Ti or Cu-Mo), R_{SEM} is the semiconductor resistance, and R_C is the contact resistance. On the right side of this equation R_M is totally negligible compared with the two other components. If we draw the total resistance versus the distance between the lines, the steep shows R_{SEM} and the intersection with the vertical axis gives R_C. We have checked the results for R_{SEM} with those obtained from a four-point-probe measurement for the confirmation of the TLM data.

RESULTS AND DISCUSSION

Fig. 3 shows the variation of contact resistance with different thickness ratios for Ti to Cu. By choosing a very small ratio between the thicknesses, it will be possible for the Cu to diffuse through the barrier and deteriorate the contact and substrate conditions. In addition, Ti will not be able to play its normal role; i.e. making a silicide or a high quality ohmic contact with the poly-crystalline silicon. On the other hand, the ratio must be kept under some threshold; otherwise the contact resistance will be increased. We have observed that a suitable ratio is about 11/89 and choosing it below 5/95 is very unfavorable. Fig. 3 also shows the linear relationship between the resistance and the distance for each case. From this relationship and by considering the area of the relevant contact we have calculated the special contact resistance to be 9.72×10^{-6} Ω-cm^2. The annealing temperature in this case was 300 °C. The change of the ratio doesn't have any significant effect on the semiconductor resistance. This fact shows that the diffusion of the Cu has been hampered successfully by these thicknesses of Ti. A similar process has been done for Cu-Mo structure and the results are shown in Fig. 4. It is obvious that the special contact resistance has a lower value, which is about 8.58×10^{-6} Ω-cm^2.

The next important parameter is the annealing temperature. In Figs. 5 and 6, the I-V curves of the ohmic contacts at different annealing temperatures for Cu-Mo and Cu-Ti have been shown respectively. By increasing the temperature from 200 °C, the current increases and the resistance decreases. However, as the temperature rises above 400 °C, many practical problems begin to happen for the metals; for example the contamination of the

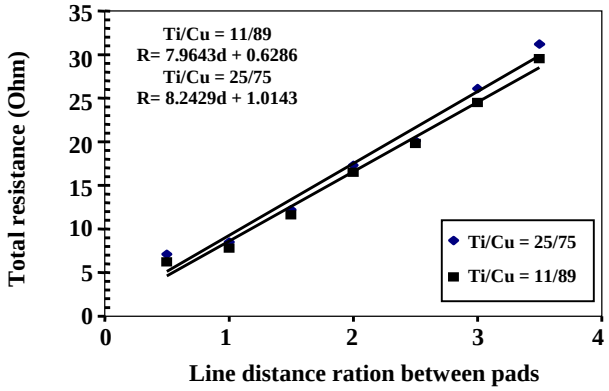


Fig. 3: Variation of the total contact resistance with the distance between TLM lines for two different Ti/Cu thickness ratio annealed at the temperature of 350 °C. R_C and R_{SEM} can be extracted from the line equations that have been shown in the of the figure.

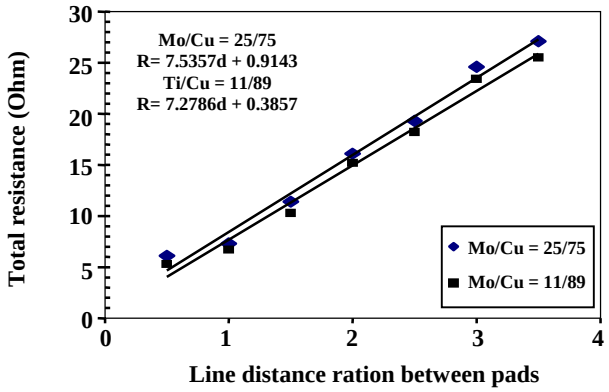


Fig. 4: Variation of the total contact resistance with the distance between TLM lines for two different Mo/Cu thichness ratio annealed at the temperature of 350 °C. As can be seen, Mo has lower resistance than Ti.

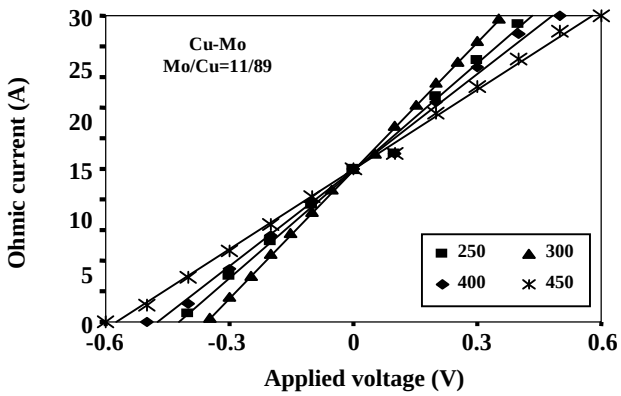


Fig. 5: Total current versus the applied voltage for the ohmic contacts with different annealing temperatures for Cu-Mo structure. An optimum temperature of about 300 °C has been obtained.

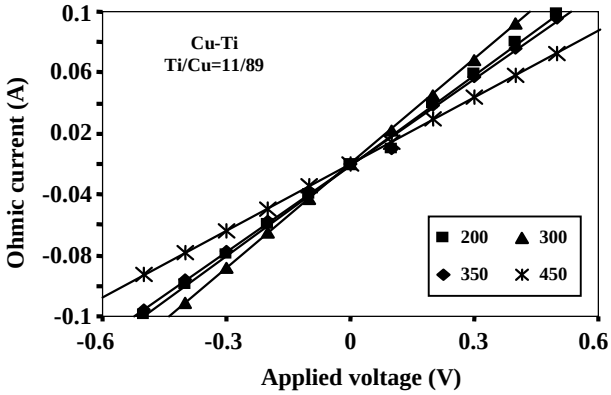


Fig. 6: Total current versus the applied voltage for the ohmic contacts with different annealing temperatures for Cu-Ti structure. An optimum temperature of about 300 °C has been obtained.

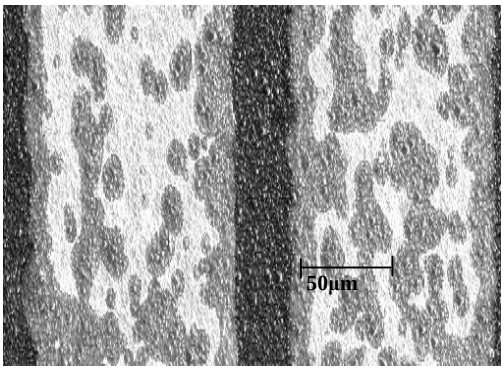


Fig. 7: SEM image of the alloys which have been annealed above 450 °C. As can be seen, due to the high diffusivity of the Cu atoms, Cu has passed Ti or Mo film and has reached to the silicon substrate.

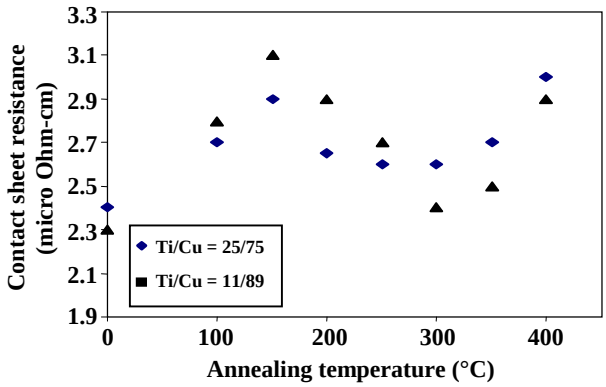


Fig. 8: Contact sheet resistance versus the annealing temperature for Cu-Ti structures with different Ti/Cu thickness ratios. A local minimum sheet resistance can be observed at about 250 °C- 300 °C.

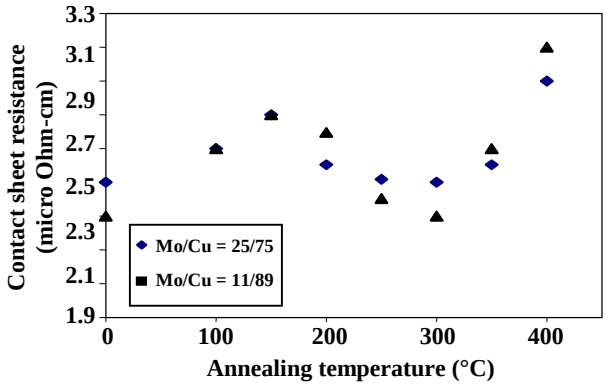


Fig. 9: Contact sheet resistance versus the annealing temperature for Cu-Mo structures with different Mo/Cu thickness ratios. A local minimum sheet resistance can be observed at about 300 °C.

distribution barrier of Si-Ti or Si-Mo by Cu. 500°C is the above limit for the annealing process and above this temperature much instability in the structure were observed. Fig. 7 shows a section of TLM structure of a sample annealed a temperature of 450 °C a large volume of Cu has diffused into the wafer and so cancelled the positive function of the Ti.

Not only the temperature affects the contact resistance, but also it determines the transmission line sheet resistance, which is an important factor when considering the total resistance of the cells contacts [8]. Figs. 8 and 9 show the sheet resistance of the alloy layers of Cu-Ti and Cu-Mo with two different thicknesses of metal versus the temperature. Without any heat treatment, the resistance is the one of the Cu layer. At the temperatures above 100 °C, formation of the alloy begins and the resistance increases.

However, at higher temperatures when a high quality alloy forms, the resistance reaches its initial values.

Experimental data shows that the selection of temperatures between 250-300 °C lead to a reasonable value for the sheet resistance, which is in agreement with our selection of 300 °C for having a low specific contact resistance.

The last parameter considered here is the duration of the annealing process. The study reveals that for having a rapid alloy formation, the samples must be annealed at least for 10 minutes and the best time is about 18 minutes. As the annealing temperature decreases, the annealing time must be increased for achieving a satisfactory result.

CONCLUSIONS

Cu-Mo and Cu-Ti structures were fabricated on multi-crystalline silicon substrates to optimize a very low-resistance ohmic contact for solar cell applications. The results showed specific contact resistance of 8.58×10^{-6} Ω-cm^2 and 9.72×10^{-6} Ω-cm^2 and transmission line sheet resistance of 2.3×10^{-6} Ω-cm and 2.4×10^{-6} Ω-cm for Mo and Ti as the underlying metals respectively. Effects of post annealing treatments on the specific contact resistance and the quality of contacts were studied. It has been observed that the annealing temperature of 300 °C is suitable to obtain an effective contact with perfect adhesion, while annealing at temperatures above 400 °C results in Cu diffusion through the Mo or Ti barriers into the silicon and degradation of contact quality.

Furthermore, contacts with different thickness ratios were fabricated and examined to obtain the optimum contact structure. The optimum thickness ratios of 10/90 and 13/87 achieved for Cu-Mo and Cu-Ti contact systems. Conclusively, the Cu-Mo structure was chose due to due to its good adhesion, lower special resistance and instinct characteristic of being a better barrier for hampering the Cu diffusion.

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